

What are Single Event Effects?

Single Event Effects are caused by a single, energetic particle which can originate from the ions in a cosmic ray (galactic or solar in origin) or from a high energy proton. Two major types of Single Event Effects are described below; Single Event Upsets (SEU) are considered soft-errors and are non-destructive. Single Event Latchups (SEL) are hard errors and can be potentially destructive to the device.

Single Event Upset, SEU

Single Event Upset, SEU, is the radiation-induced upset of a logic gate, converting a zero to a one or vice versa. It is generally temporary, and can be corrected by rewriting to that logic gate. It can be highly problematic when in control paths, but can be corrected when in data path. SEU is measured in either LET (sensitivity vs. energy) or errors per bit day (e/bd), measuring overall likelihood of an upset in a given device in a single day.

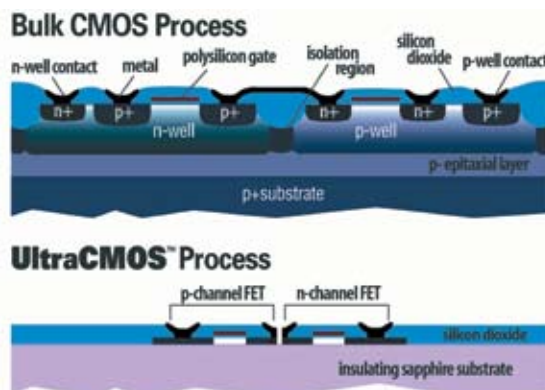
Single Event Latchup, SEL

Single Event Latchup, SEL, is the radiation-induced latchup of a CMOS logic gate. This can happen when a high energy particle strikes the parasitic thyristor inherent to Bulk CMOS designs and causes a short circuit from power to ground within the device. It is often catastrophic and results in permanent damage, requiring at a minimum power-down to recover. However, products created using the UltraCMOS™ (silicon on sapphire, SOS) technology process do not contain the bulk parasitics found in regular CMOS devices, making latchup impossible on SOS technology.

Single Event Effects in UltraCMOS™ Devices

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Figure 1. Bulk CMOS process vs UltraCMOS Process. The Bulk Parasitics which cause SEL are eliminated in the UltraCMOS process, making latchup impossible.



Custom RH PLL SEU Results

- Small Cross-Section for Phase Errors, $1E-5/cm^2$ @ LET=40
- Negligible Cross-Section For Frequency Errors, $1E-9$ derives from experimental limitations (moderate fluence w/ no upsets)
- Frequency Error Rate Indicates SEE Resistance Of Digital Logic;
- Phase Error Rate Indicates SEE Sensitivity Of Linear Circuitry, Low Voltage Swing / High Speed Prescalers.

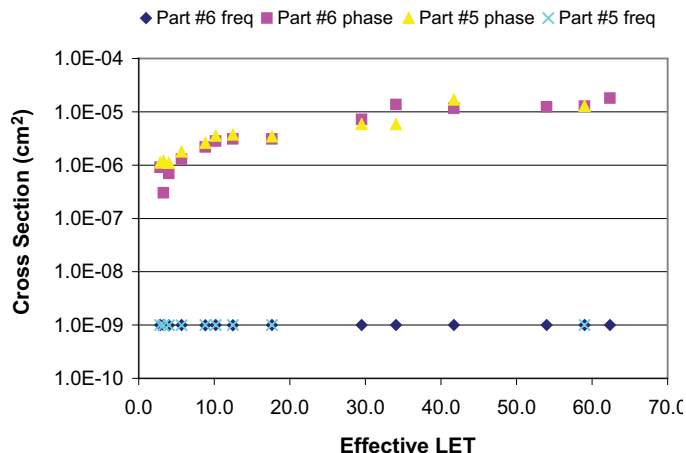


Figure 2. Peregrine 4N50 Cross Section

3GHz PLL SEU Test Results

- Small Cross-Section for Phase Errors, $3E-5/cm^2$ @ LET=40
- Negligible Cross-Section For Frequency Errors, $5E-10$ derives from experimental limitations (moderate fluence w/ no upsets). Logic (Frequency) LET Threshold = $52MeV-cm^2/mg$
- Frequency Error Rate Indicates SEE Resistance Of Digital Logic;
- Phase Error Rate Indicates SEE Sensitivity Of Linear Circuitry, Low Voltage Swing / High Speed Prescalers.

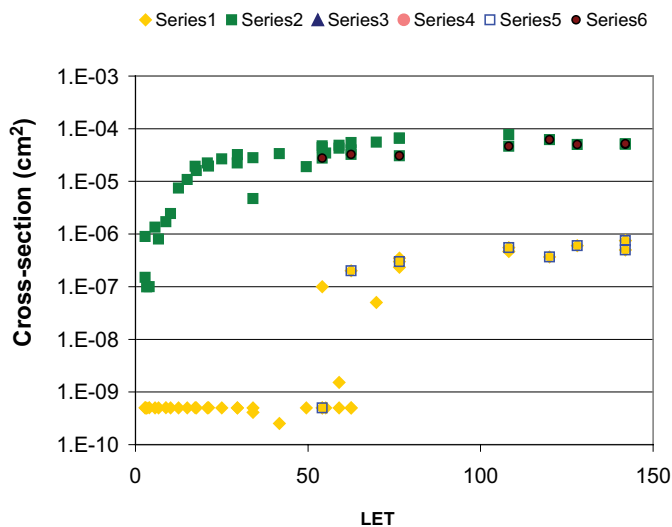


Figure 3. Frequency and Phase Cross-section vs LET

SEU Summary for UltraCMOS devices

Logic Upset Threshold Is Very High on PLLs

- LET>60 (no upsets) On Custom Design
- LET>52 on 3GHz Space Standard Product
- Negligible Cross-Sections

Phase Upset Threshold Is Low (Proton)

- Proton cross-sections in $1E-7$ cm² range, Saturated cross-sections of $1E-5$ cm² (2GHz), $3E-5$ cm² (3GHz)
- Phase Errors Are Self-Recovering
- Higher-Speed Design Is More Sensitive (Natural

Consequence Of Reducing Node Capacitance And Increasing Bandwidth)

Other products will behave similarly

- PE 9301/2/3/4/8 & I/O have both logic & phase upset, but transistor count is ~10X less, so expect ~10X better SEU
- Mixers, DSA's, switches and most other products have only logic upsets since no source-controlled-logic